Fig. 1

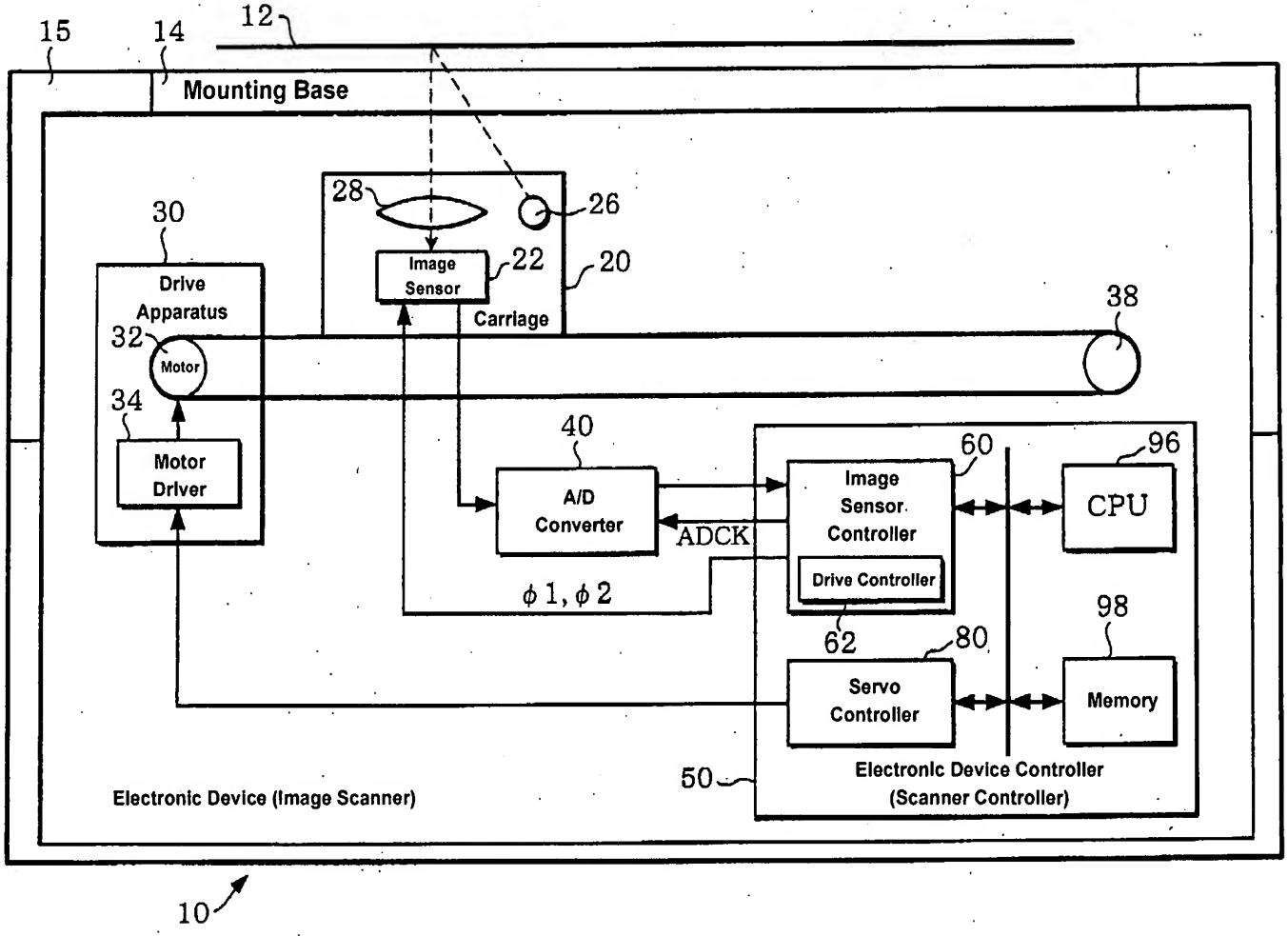

15
14
12
Mounting Base
28
26
30
Image Sensor
22
20
Drive Apparatus
Carriage
38
32
Motor
34
Motor Driver
40
A/D Converter
ADCK
60
Image Sensor Controller
Drive Controller
96
CPU
φ1, φ2
98
62
80
Servo Controller
Memory
50
Electronic Device Controller (Scanner Controller)
Electronic Device (Image Scanner)
10

Fig. 2 (A)

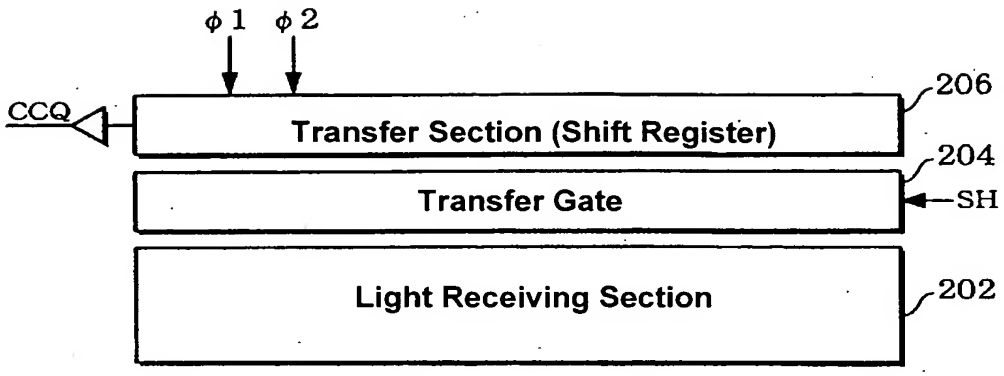


Fig. 2 (B)

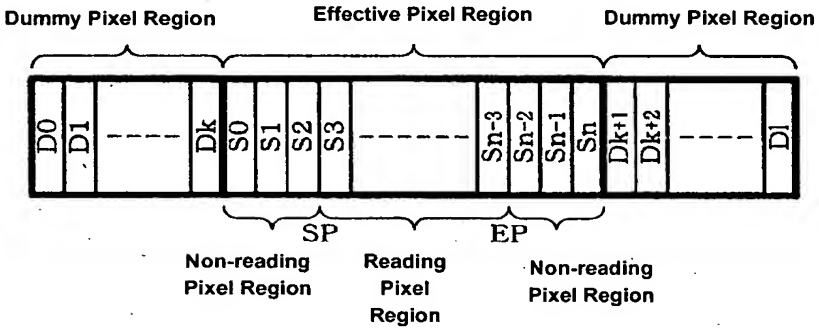


Fig. 2 (C)

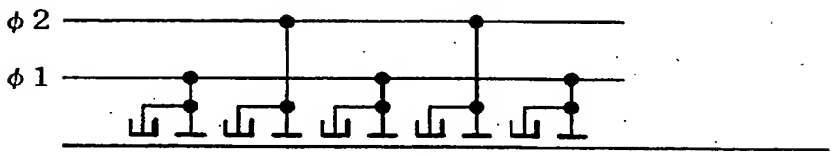


Fig. 3 (A)

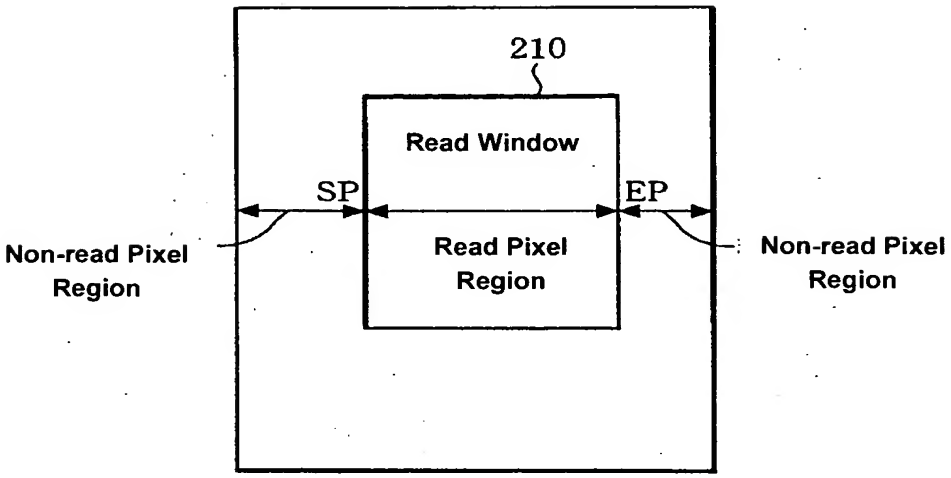

210
Read Window
SP
EP
Non-read Pixel Region
Read Pixel Region
Non-read Pixel Region

Fig. 3 (B)

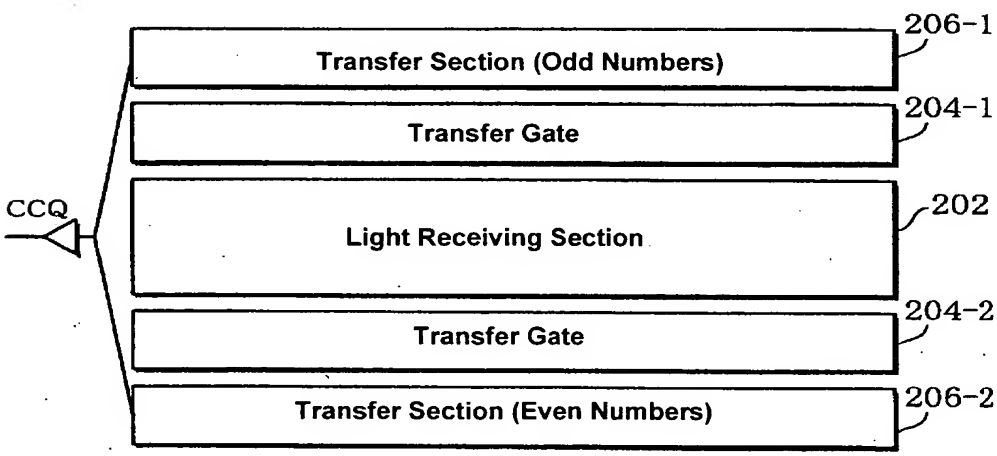

206-1
Transfer Section (Odd Numbers)
204-1
Transfer Gate
CCQ
202
Light Receiving Section
204-2
Transfer Gate
206-2
Transfer Section (Even Numbers)

Fig. 4 (A)

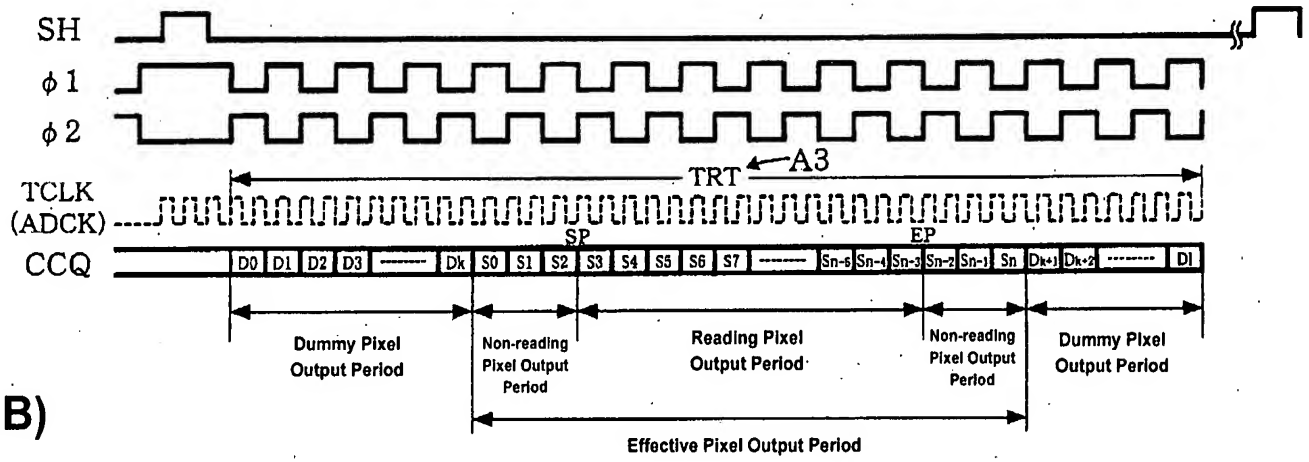

SH
ϕ1
ϕ2
TCLK
(ADCK)
CCQ
A3
TRT
SP
EP
D0 D1 D2 D3 ------- Dk S0 S1 S2 S3 S4 S5 S6 S7 ------- Sn-6 Sn-4 Sn-3 Sn-2 Sn-1 Sn Dk+1 Dk+2 ------- Dl
Dummy Pixel Output Period
Non-reading Pixel Output Period
Reading Pixel Output Period
Non-reading Pixel Output Period
Dummy Pixel Output Period
Effective Pixel Output Period

Fig. 4 (B)

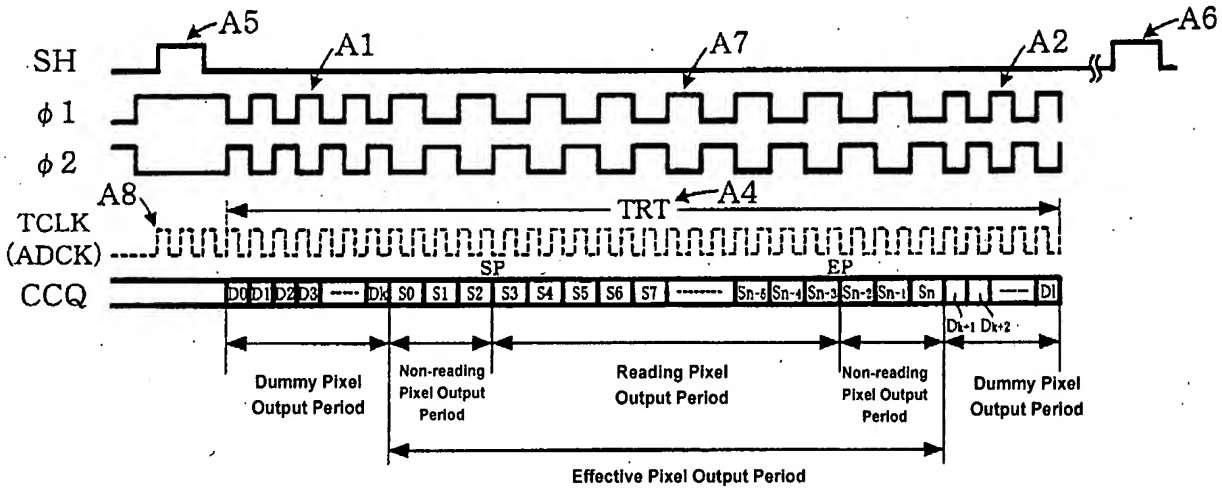

A5
A1
A7
A2
A6
SH
ϕ1
ϕ2
A8
A4
TRT
TCLK
(ADCK)
CCQ
SP
EP
D0 D1 D2 D3 ---- Dk S0 S1 S2 S3 S4 S5 S6 S7 ------- Sn-6 Sn-4 Sn-3 Sn-2 Sn-1 Sn Dk-1 Dk+2 ---- Dl
Dummy Pixel Output Period
Non-reading Pixel Output Period
Reading Pixel Output Period
Non-reading Pixel Output Period
Dummy Pixel Output Period
Effective Pixel Output Period

Fig. 5 (A)

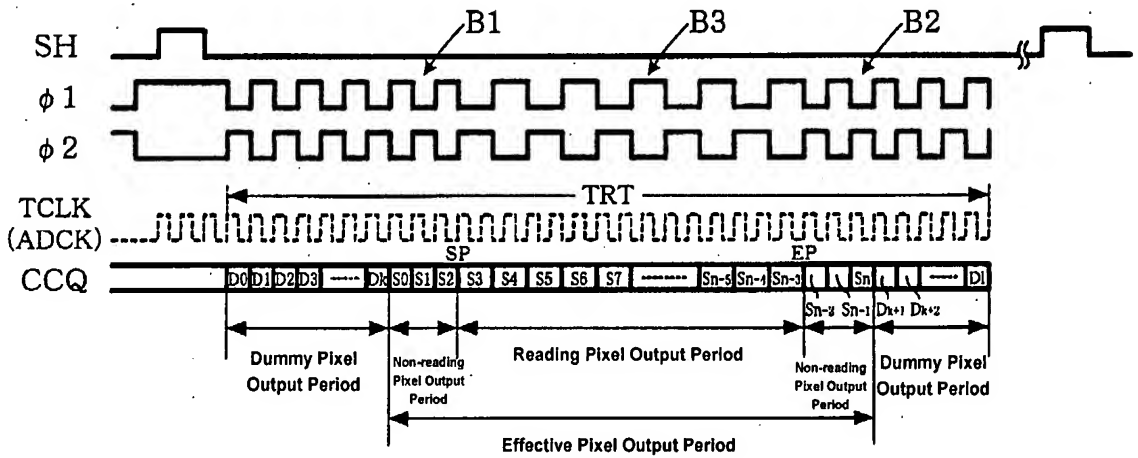

SH
B1
B3
B2
ϕ1
ϕ2
TRT
TCLK
(ADCK)
SP
EP
CCQ
D0 D1 D2 D3 ---- Dk S0 S1 S2 S3 S4 S5 S6 S7 ---- Sn-5 Sn-4 Sn-3 Sn-2 Sn-1 Sn Dk+1 Dk+2 ---- D1
Dummy Pixel Output Period
Non-reading Pixel Output Period
Reading Pixel Output Period
Non-reading Pixel Output Period
Dummy Pixel Output Period
Effective Pixel Output Period

Fig. 5 (B)

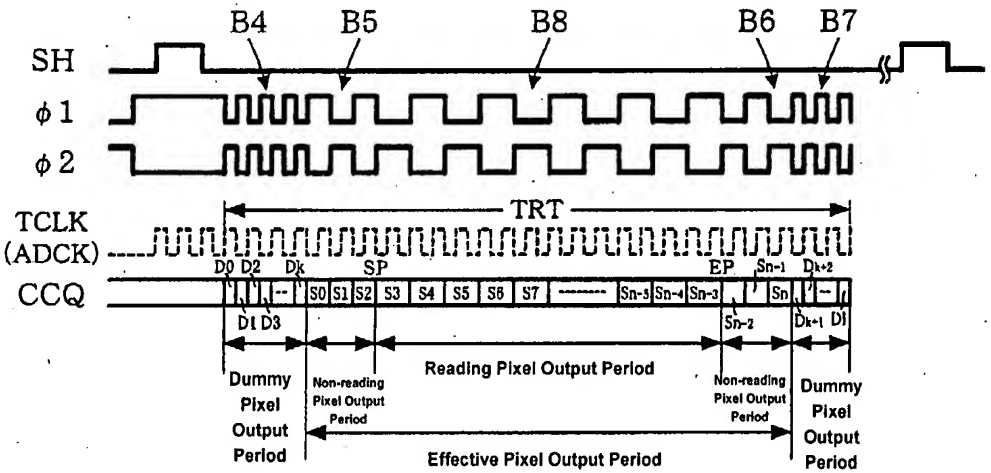

SH
B4
B5
B8
B6
B7
ϕ1
ϕ2
TRT
TCLK
(ADCK)
CCQ
D0 D2 Dk SP EP Sn-1 Dk+2
S0 S1 S2 S3 S4 S5 S6 S7 ---- Sn-5 Sn-4 Sn-3 Sn
D1 D3
Sn-2
Dk+1 D1
Dummy Pixel Output Period
Non-reading Pixel Output Period
Reading Pixel Output Period
Non-reading Pixel Output Period
Dummy Pixel Output Period
Effective Pixel Output Period

Fig. 6

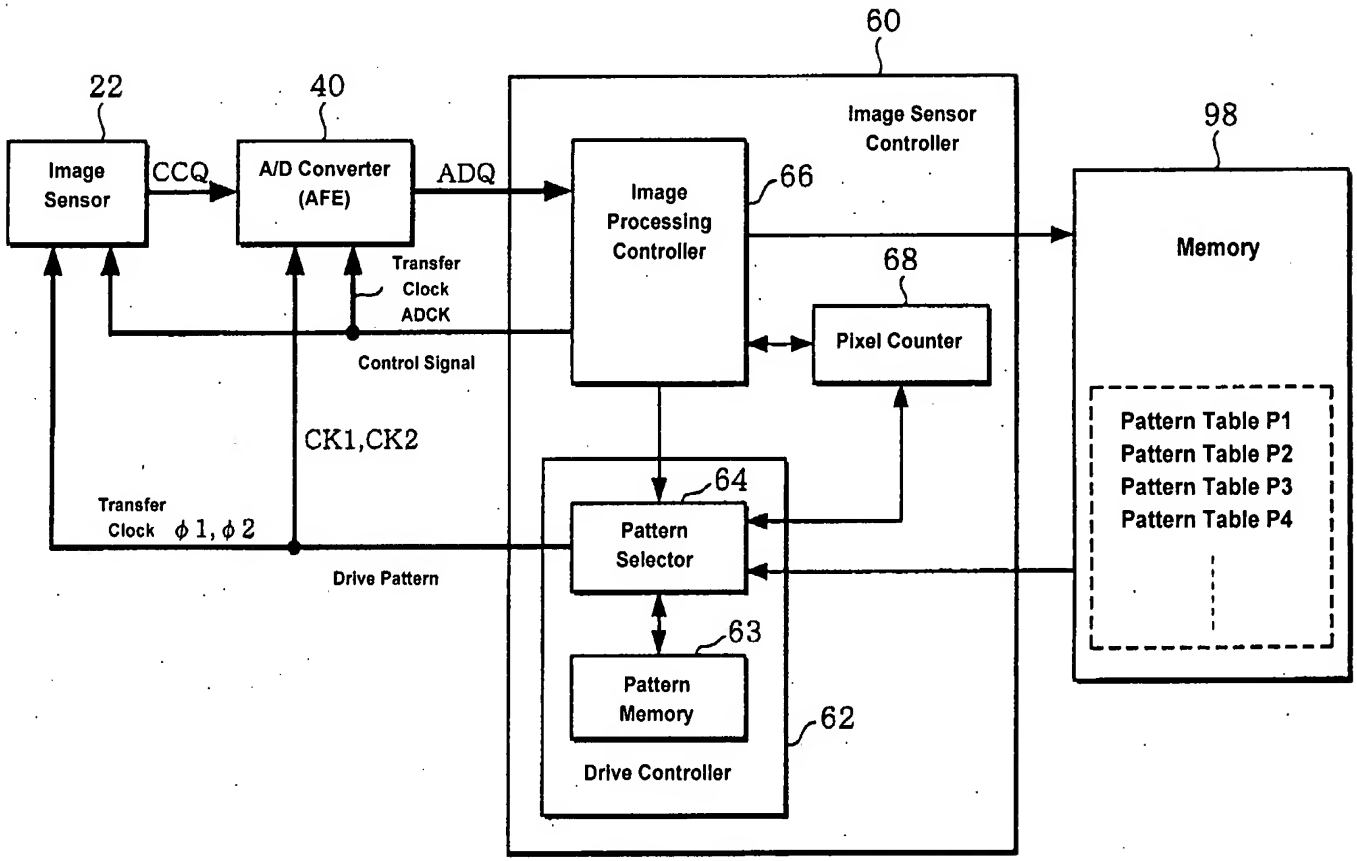

60
22
40
Image Sensor Controller
98
Image Sensor
CCQ
A/D Converter (AFE)
ADQ
Image Processing Controller
66
Memory
Transfer Clock ADCK
68
Pixel Counter
Control Signal
CK1,CK2
Pattern Table P1
Pattern Table P2
Pattern Table P3
Pattern Table P4
64
Transfer Clock φ1, φ2
Pattern Selector
Drive Pattern
63
Pattern Memory
62
Drive Controller

Fig. 7

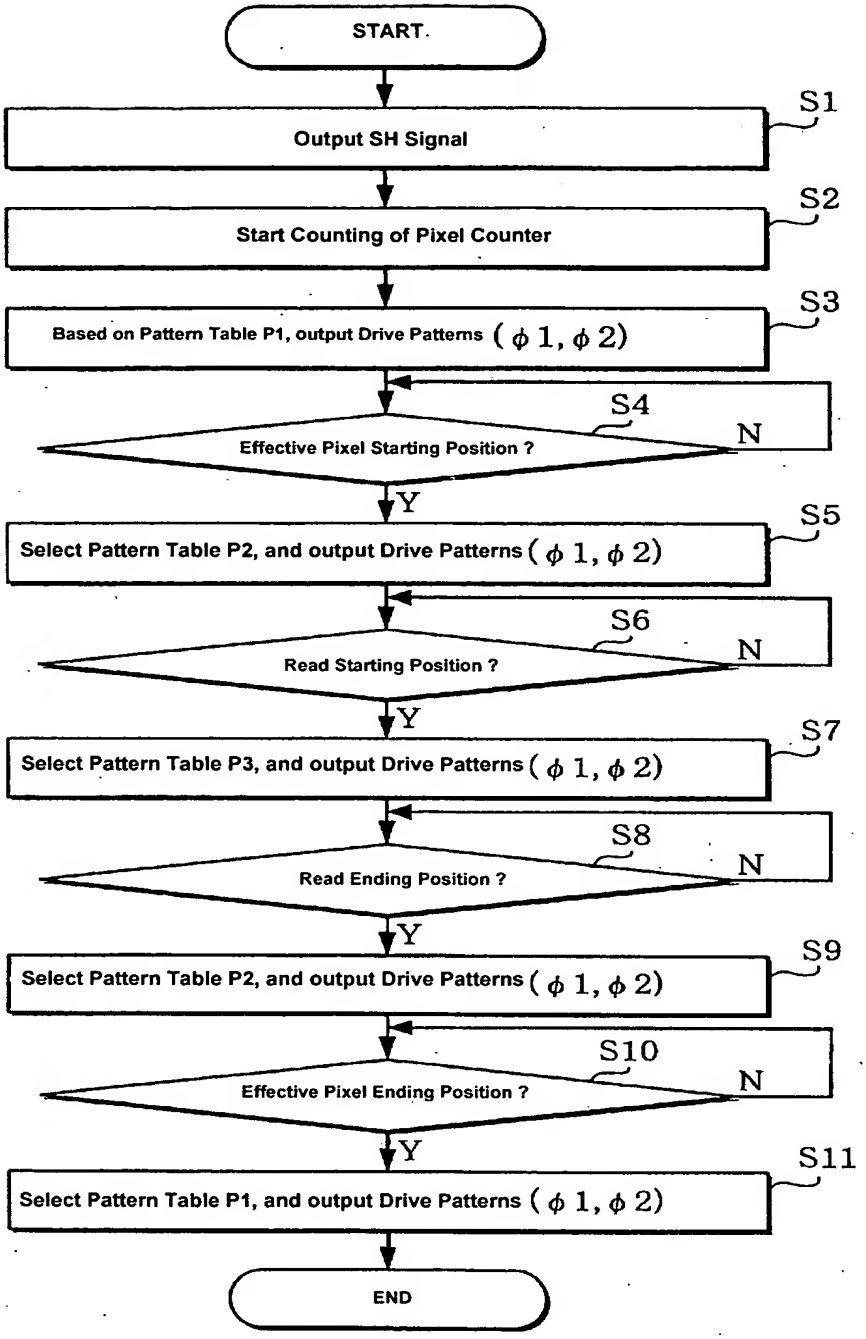

START
Output SH Signal
S1
Start Counting of Pixel Counter
S2
Based on Pattern Table P1, output Drive Patterns (φ 1, φ 2)
S3
Effective Pixel Starting Position ?
S4
N
Y
Select Pattern Table P2, and output Drive Patterns (φ 1, φ 2)
S5
Read Starting Position ?
S6
N
Y
Select Pattern Table P3, and output Drive Patterns (φ 1, φ 2)
S7
Read Ending Position ?
S8
N
Y
Select Pattern Table P2, and output Drive Patterns (φ 1, φ 2)
S9
Effective Pixel Ending Position ?
S10
N
Y
Select Pattern Table P1, and output Drive Patterns (φ 1, φ 2)
S11
END

Fig. 8 (A)

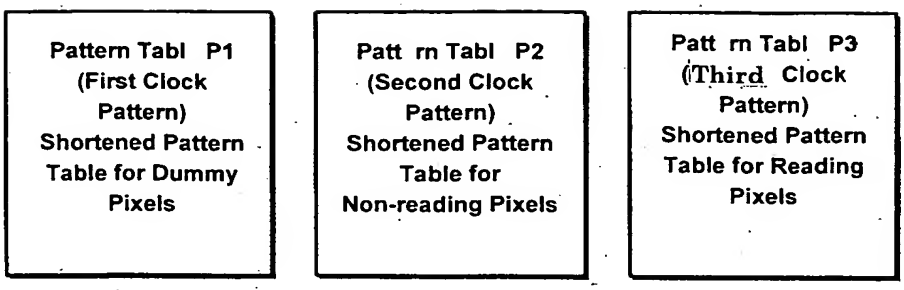


Fig. 8 (B)

Pattern Table

ADR	ϕ1	ϕ2	----
00	0	0	
01	1	0	----
02	1	0	
03	1	0	
04	0	0	----
05	0	1	
06	0	1	
07	0	1	----
08	0	0	
09	0	0	

Fig. 8 (C)

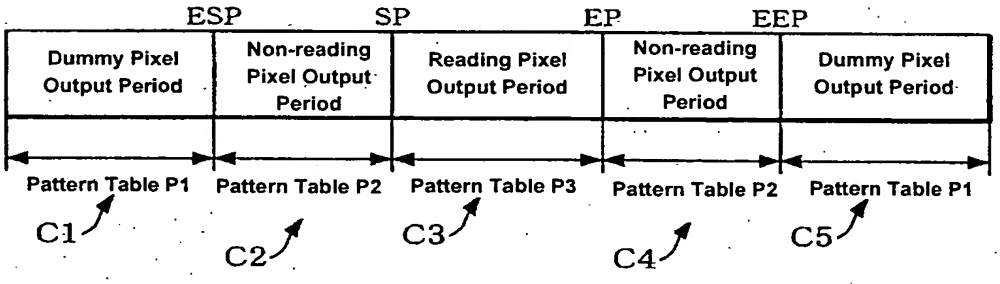


Fig. 8 (D)

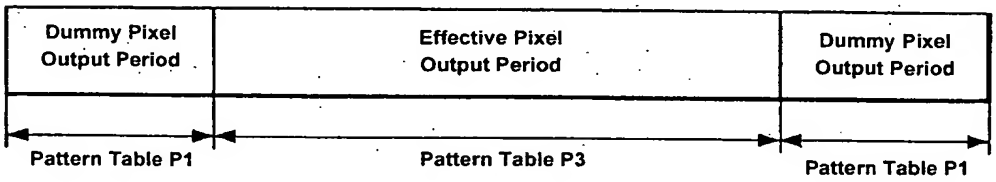


Fig. 9 (A)

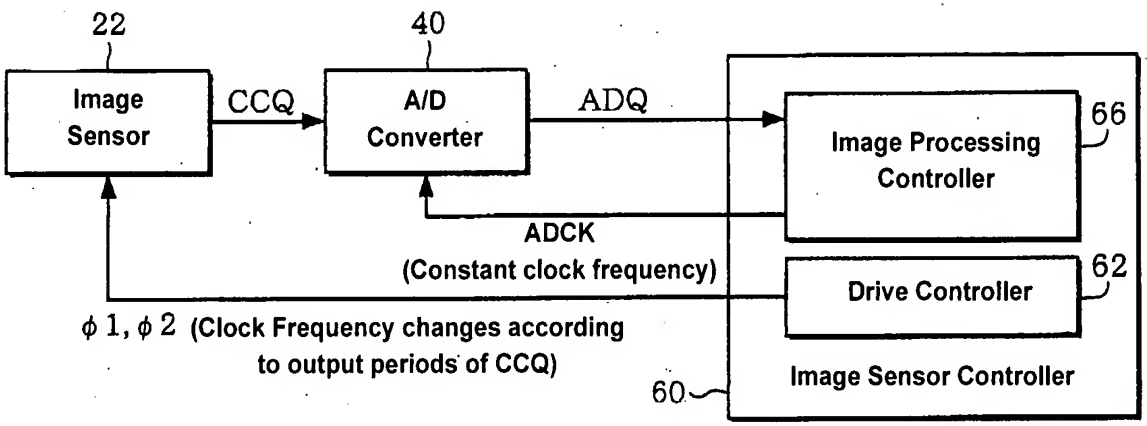


Fig. 9 (B)

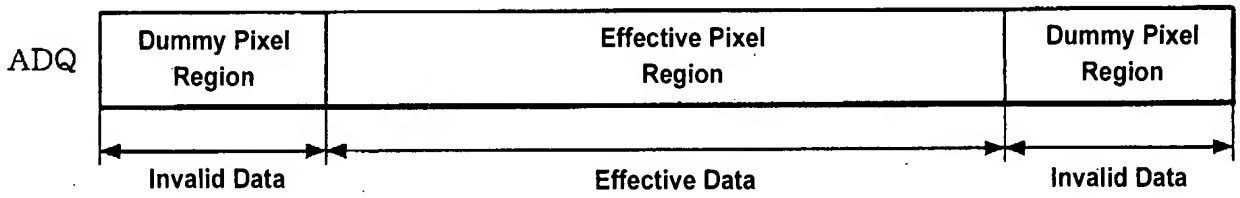


Fig. 9 (C)

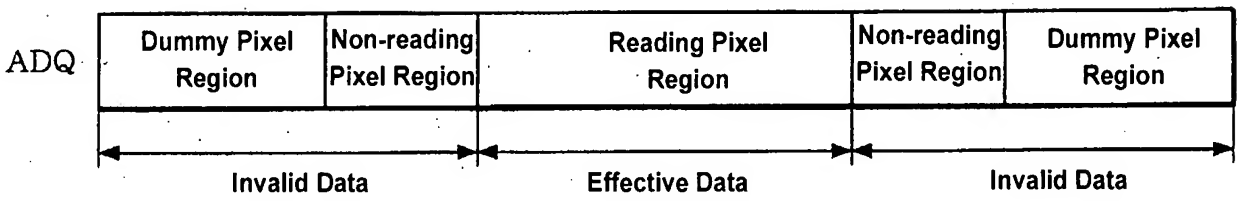


Fig. 10

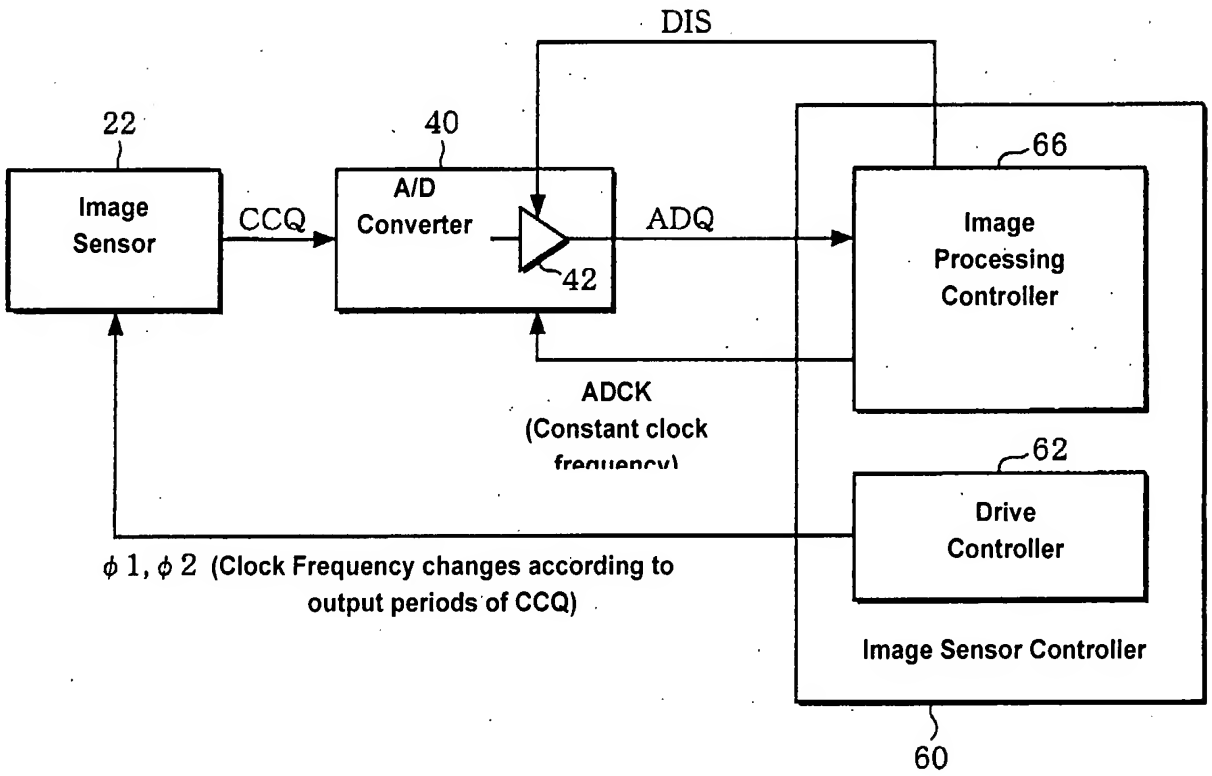
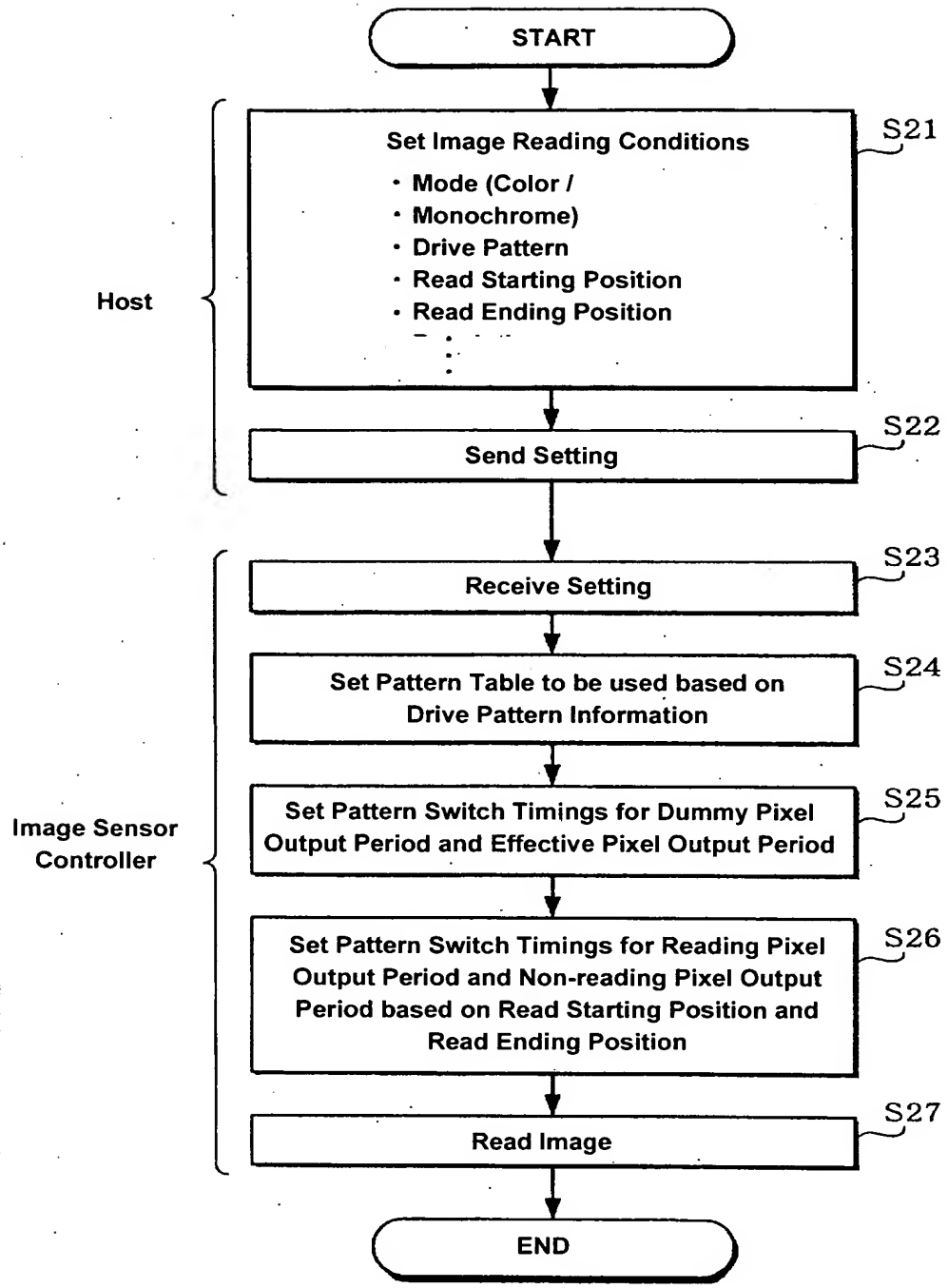

DIS
22
40
66
Image Sensor
CCQ
A/D Converter
ADQ
42
Image Processing Controller
ADCK
(Constant clock
62
Drive Controller
ϕ 1, ϕ 2 (Clock Frequency changes according to output periods of CCQ)
Image Sensor Controller
60

Fig. 11


START
Host
Set Image Reading Conditions
• Mode (Color /
• Monochrome)
• Drive Pattern
• Read Starting Position
• Read Ending Position
S21
Send Setting
S22
Image Sensor Controller
Receive Setting
S23
Set Pattern Table to be used based on Drive Pattern Information
S24
Set Pattern Switch Timings for Dummy Pixel Output Period and Effective Pixel Output Period
S25
Set Pattern Switch Timings for Reading Pixel Output Period and Non-reading Pixel Output Period based on Read Starting Position and Read Ending Position
S26
Read Image
S27
END

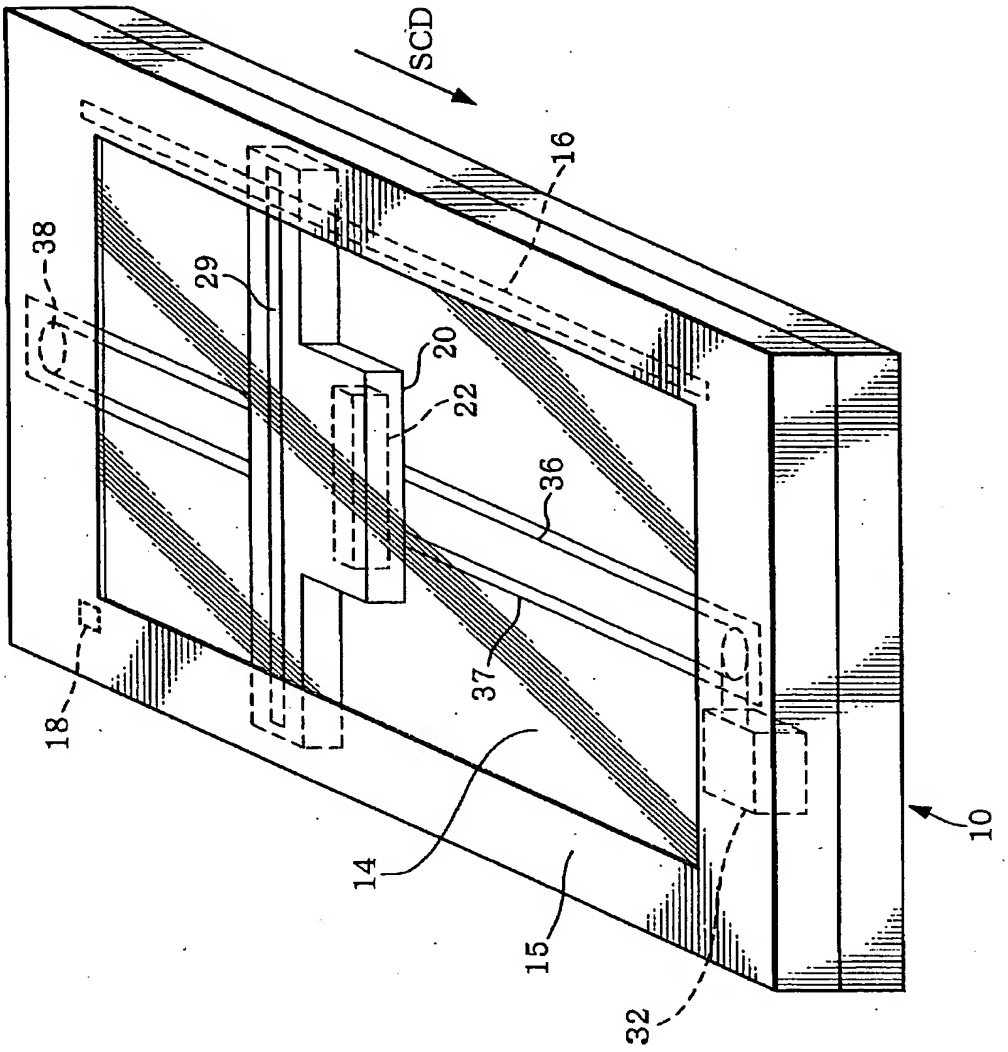


Fig. 12

Fig. 13

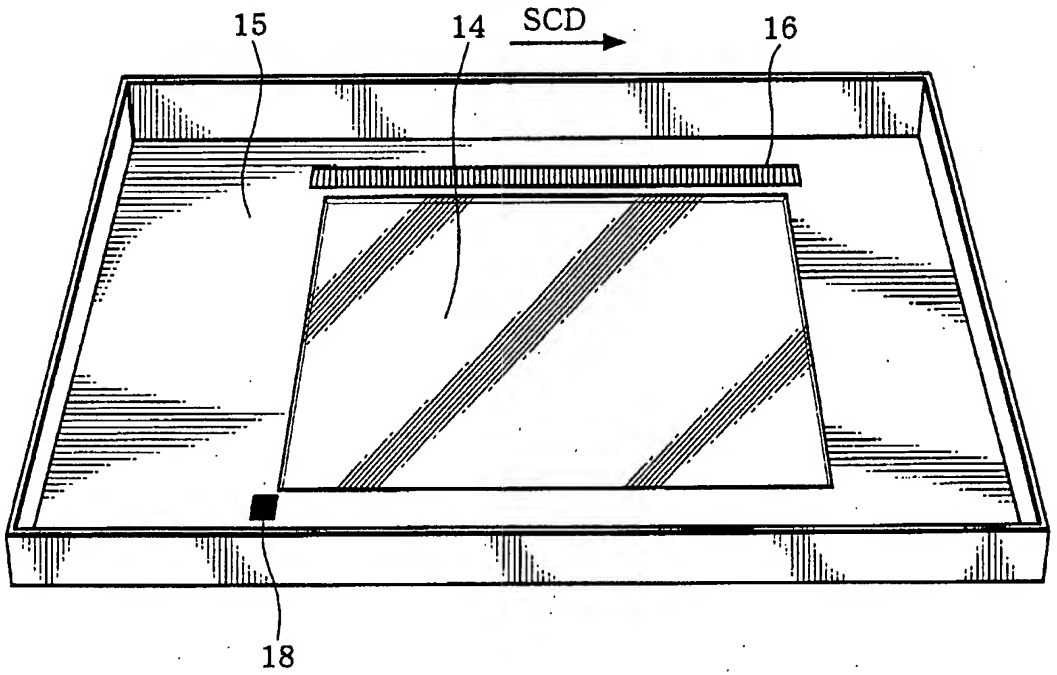


Fig. 14 (A)

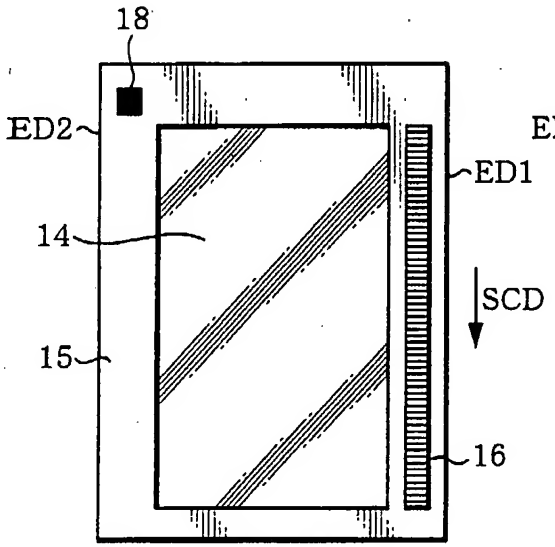


Fig. 14 (B)

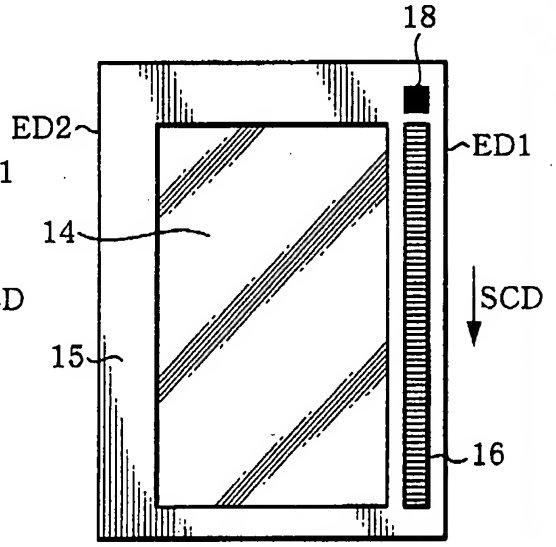


Fig. 14 (C)

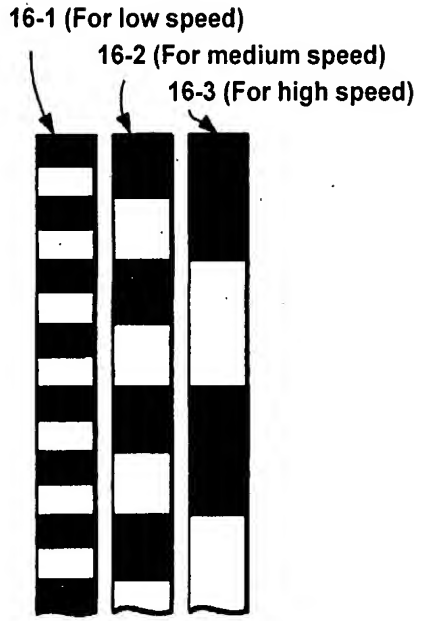


Fig. 15

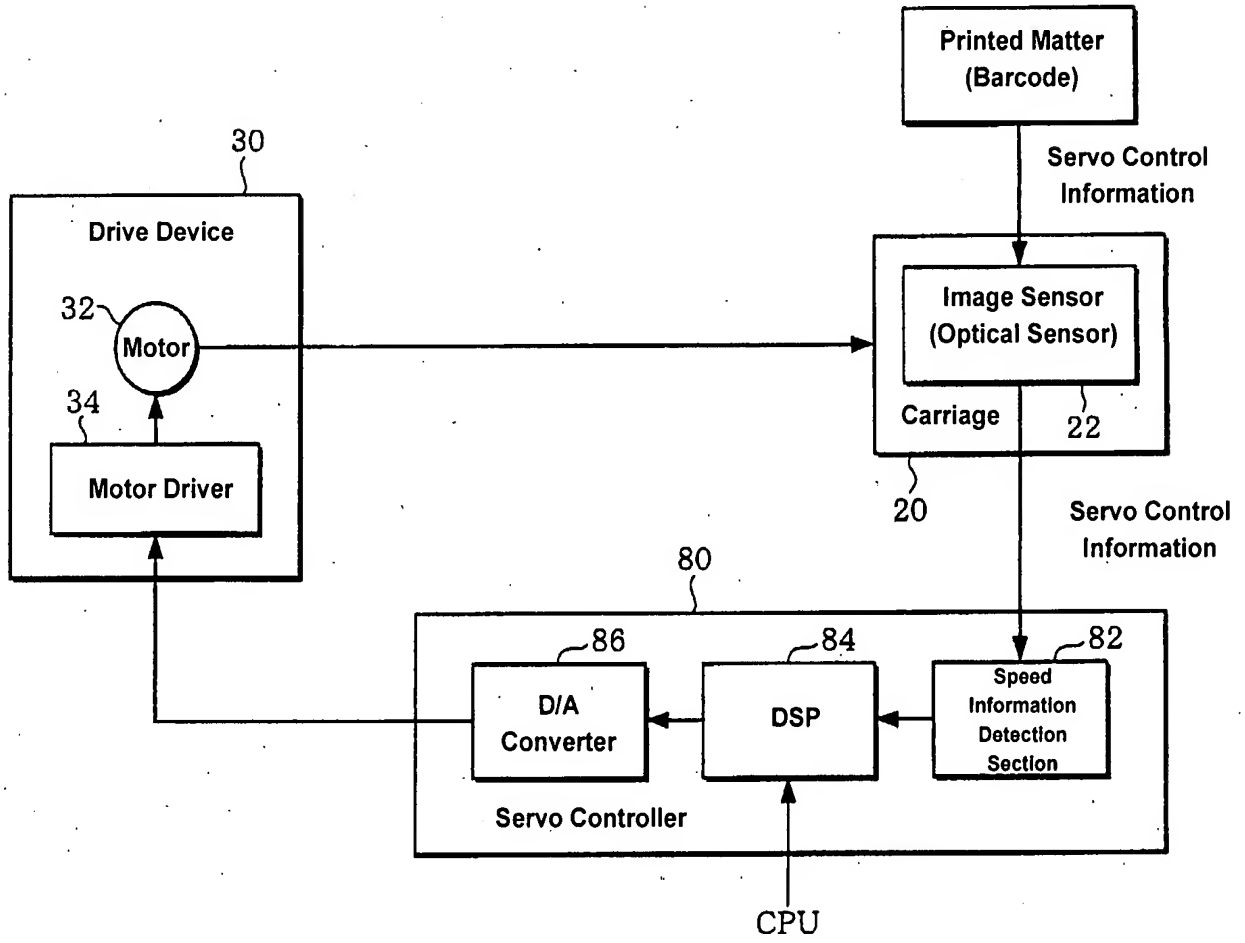
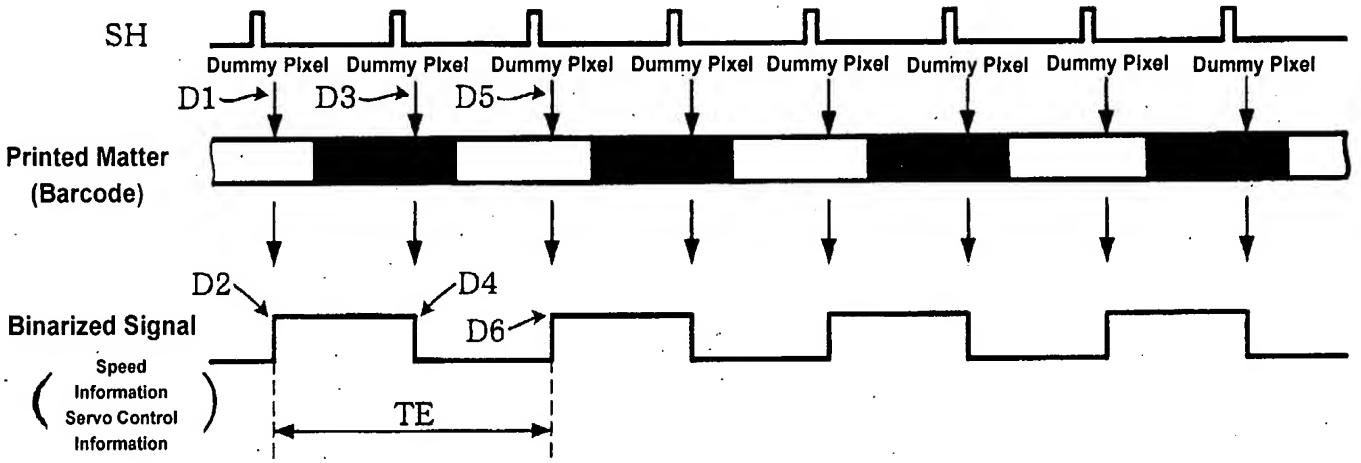

Printed Matter
(Barcode)
Servo Control
Information
30
Drive Device
32
Motor
34
Motor Driver
Image Sensor
(Optical Sensor)
Carriage
22
20
Servo Control
Information
80
86
84
82
D/A
Converter
DSP
Speed
Information
Detection
Section
Servo Controller
CPU

Fig. 16


SH
Dummy Pixel
Dummy Pixel
Dummy Pixel
Dummy Pixel
Dummy Pixel
Dummy Pixel
Dummy Pixel
Dummy Pixel
D1
D3
D5
Printed Matter
(Barcode)
D2
D4
D6
Binarized Signal
Speed
Information
Servo Control
Information
TE